High-Power Pulsed UHF and *L* Band p^+-n-n^+ Silicon TRAPATT Diode Lasers

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Abstract—**The design and performance of both the lumped-element TRAPATT oscillator circuit and deep-diffused p^+-n-n^+ silicon TRAPATT diodes designed primarily for pulsed radar applications in the UHF and *L* band frequency ranges are discussed. Circuit conditions for optimum performance are described. Methods of optimizing diodes are presented. Diode performance capability is shown to depend on the relative position of the junction in the device depletion region. Peak powers close to 900 W and maximum conversion efficiencies of 40 percent have been achieved from diodes with large p-region width to total depletion region width ratios. RF leading-edge jitter of less than 1 ns has been obtained under optimum circuit and diode operating conditions.**

I. INTRODUCTION

HIGH-POWER high-efficiency silicon TRAPATT diodes are potentially useful as solid-state sources for fuses, IFF transponder systems, and for phased array radar systems [1]–[3]. For some pulsed radar applications, high-efficiency high-power TRAPATT oscillators operating under low duty and short pulsed conditions are required. In addition, small size, low cost, and high-quality spectral output are some of the prime circuit design requirements. In this paper, the design and performance of pulsed lumped-element TRAPATT oscillators utilizing deep-diffused p^+-n-n^+ silicon TRAPATT diodes and designed primarily for solid-state pulsed radar applications in the UHF and lower *L* band frequency ranges will be discussed. Experimental results on some of the factors affecting efficient operation of lumped-element TRAPATT oscillator circuits will be presented.

Until recently, most attention on higher power generation from p^+-n-n^+ silicon TRAPATT devices has been concentrated on diodes with abrupt junctions. However, most successful TRAPATT diodes at frequencies below 5 GHz have utilized graded junctions where an appreciable part of the junction electric field extends into the p-side of the junction. A graded junction will have varying portions of the depletion width extending into the p-side of the junction depending on material parameters and diffusion conditions. Although several studies [4]–[6] have been reported on the high-power generation from graded p^+-n-n^+ silicon TRAPATT structures, the peak powers achieved from these single devices have been considerably less than 500 W. Furthermore, little or no attention has been paid to the enhancement of the power capability of these structures by exploiting the relative position of the junction in the device depletion region. The observed dependence of the performance capability of deep-diffused p^+-n-n^+ silicon TRAPATT diodes on the width ratio (p-region width/total depletion region width, W_P/W_T) and the diode fabrication technique will be discussed.

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II. DEVICE CONSIDERATIONS

The high breakdown voltage ($100 < V_B \leq 300$ V), large area, and high bias current levels associated with high-power UHF/*L* band TRAPATT diodes influence the material and processing fabrication technology employed to make these devices. A typical large area high-power TRAPATT device should possess minimum material/process defects so as to minimize microplasma oscillations and low-current burnout. Therefore, it should exhibit low process-induced defects such as spikes, dislocations, and stacking faults associated with epitaxial growth [7]. In this study, deep-diffused p^+-n-n^+ silicon junction devices possessing little or none of the preceding defects have been fabricated by the pill process technology [7].

Junctions were formed by diffusing boron into arsenic-doped silicon epitaxial layers on antimony-doped n^+ substrates. Epitaxial growth and diffusions were carried out in such a way to minimize process-induced damage. Low boron surface concentrations were obtained during the diffusion process by an oxide gettering action to reduce stresses in the lattice. The resultant electrical dc junction properties have sharp breakdowns with no low-current oscillations or burnout. The electric-field and doping properties were determined by computer calculations. The diodes were mounted on gold-plated copper heatsinks solder-mounted in threaded stud packages. Fig. 1(a) shows a typical *C*–*V* profile for the case where the width ratio W_P/W_T is 0.35. It is seen that the structure is highly graded and that the measured and computed results are in excellent agreement. Note the characteristic feature of deep-diffused junctions; namely, there is no sharp definitive stage of punchthrough. Typical doping density and field profiles and width ratio for deep-diffused TRAPATT structures considered are illustrated in Fig. 1(b).

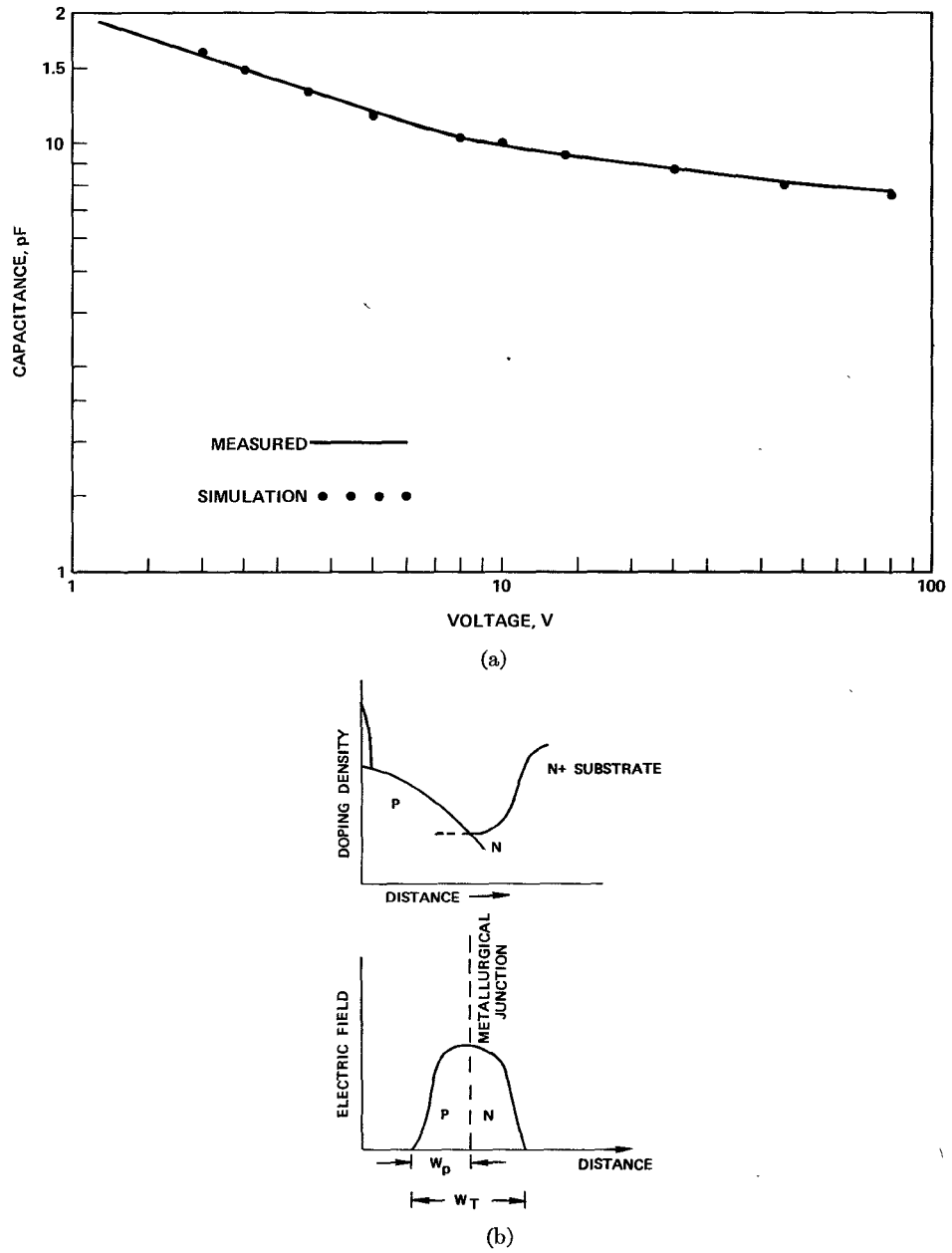


Fig. 1. (a) Typical C–V characteristics of deep-diffused TRAPATT diodes (diameter = 33 mils). (b) Typical profiles for doping density and electric field for deep-diffused TRAPATT structures (width ratio = W_P/W_T).

III. CIRCUIT CONSIDERATIONS

A. Circuit Design

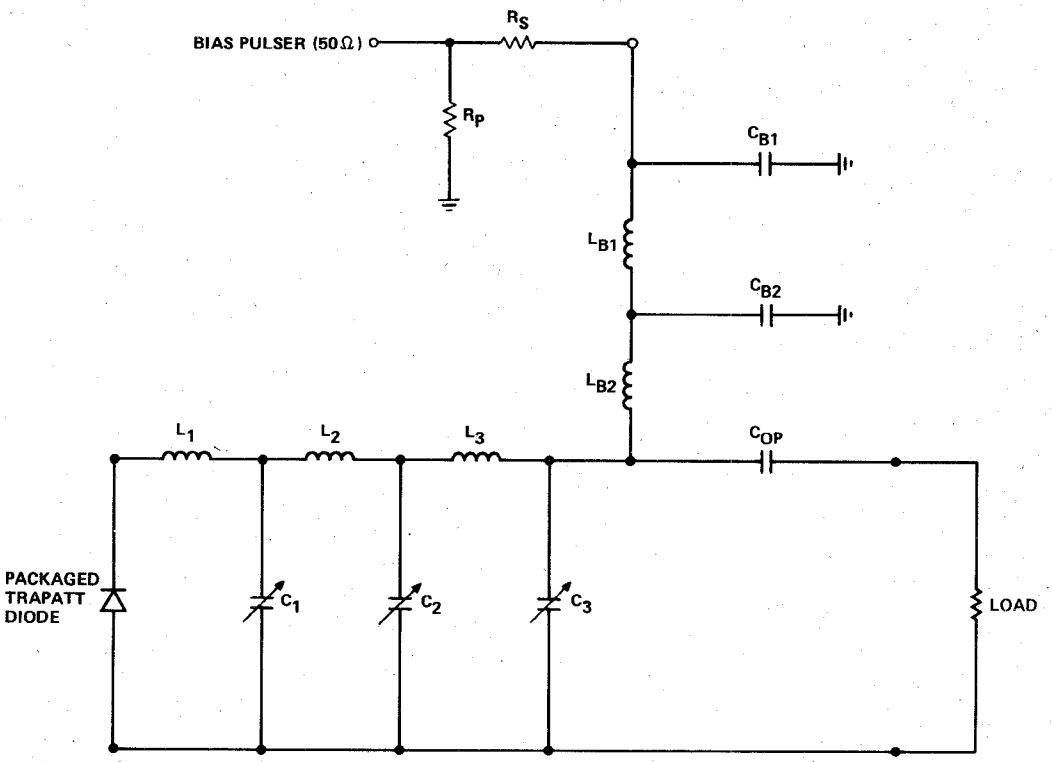
Most of the existing TRAPATT circuits have been of the distributed type basically similar to that described by Evans [8]. The operation of this type of circuit is described in terms of a wave reflected repeatedly between the diode and a filter placed approximately one-half wavelength from the diode. For UHF/L band operation, such a circuit would be rather long and cumbersome and would be unsuitable for applications where size and weight are of great importance. Thus other forms of circuitry must be found. Clorfeine *et al.* [4], by employing lumped-element circuits, have demonstrated that the distributed wave interactions phenomena are not necessary for efficient high-power TRAPATT operation. Since then, other studies [9], [10] have confirmed that high power and high efficiency are possible from lumped-element circuits with different circuit configurations. Because of the several harmonic frequencies required for efficient trapped-plasma mode oscillations, the TRAPATT circuit design necessitates proper matching of the diode behavior to that of the external circuit. An effective and simple method of achieving this is to employ a modeling technique in which both the diode and the external circuit models are described in the same form such as in time or frequency domain. The present work employed one such time-domain method—the lumped-modeling technique [11], [12]—to obtain the TRAPATT diode external circuit characterization. One of the major advantages of this method is that circuit optimization is rapid.

The criteria adopted in the circuit design are: maximum

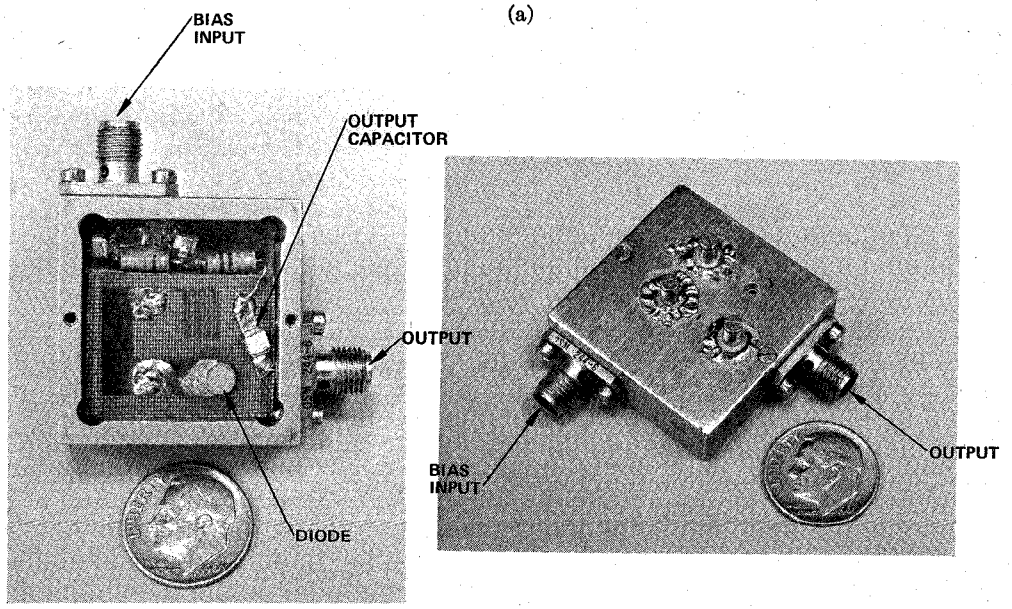
power capability consistent with optimum efficiency, a wide range of tunability with adaptability to diodes of different characteristics, simplicity, small size, and low cost.

B. Construction of Oscillator and DC Bias Circuits

Fig. 2(a) shows the schematic of the lumped-element oscillator circuit designed to meet the preceding criteria in the UHF and lower L band frequency ranges. The corresponding miniaturized operational oscillator module constructed by using integrated circuit techniques is shown in Fig. 2(b) and (c). The total circuit including the connectors has a volume of less than 0.35 in^3 and a weight of about 1 oz (in aluminum housing). The circuit series inductors L_1 (2 nH), L_2 (4.3 nH), and L_3 (32 nH) were obtained by using etched patterns on a Duroid substrate [13]–[15]. The choice of both the substrate thickness and the spacing of the etched meander patterns was such that stable inductors were obtained [13]. To ensure oscillator frequency stability, high negative temperature coefficient ceramic pad capacitors C_1, C_2, and C_3 (0.8–8 pF each) were used. These also provide the tuning necessary for optimum



(a)



(b) (c)

Fig. 2. (a) Schematic of lumped-element TRAPATT oscillator circuit plus dc bias network. (b) A miniaturized lumped-element TRAPATT oscillator module (lid removed). (c) Bottom view of oscillator module.

harmonic loading for a given diode and for the circuit adaptability to diodes of differing characteristics. Miniaturized chokes L_{B1} (51 nH), L_{B2} (100 nH), and chip capacitors C_{B1} (43 pF) and C_{B2} (68 pF) form the low-pass filter to prevent RF power leakage into the pulse circuit and to suppress any possible circuit "feedback" oscillations or bias oscillations which may deteriorate oscillator performance. C_{op} (300 pF) is the dc blocking capacitor to prevent any bias pulse from being wasted in the load. To minimize any circuit losses due to poor grounding, the Duroid substrate was soldered directly onto the circuit housing unit baseplate. The RF bias circuit is separated from the rest of the circuit to minimize any circuit interactions [7]. Fig. 2(c) is the bottom view of the circuit module showing the three tuning elements. It should be emphasized here that the choice of the optimum number of the tuning elements was not arbitrary, but was determined from both theoretical and experimental evidence satisfying the specified design criteria. A larger number of tuning elements resulted in less than 1-percent increase in efficiency with the subsequent increase in both the circuit complexity and optimization time [7]. On the other hand, a smaller number of adjustments resulted in both a decrease in circuit adaptability to different diodes and in efficiency.

The dc bias circuit consists of noninductive resistors *Rs* and *Rp* whose values were experimentally chosen to provide the necessary stable and high bias current levels needed for the large area diodes used in the tests. The circuit provides proper matching of the diode dc impedance to the 50-Ω generator output impedance. Our experiments have shown that the dc bias circuit has no effect on the oscillator RF performance provided optimum matching is obtained. We have obtained excellent results by calculating the optimum values of *Rs* and *Rp* such that the diode dc impedance presented to the dc bias circuit is $V_{\text{operating}}/I_{\text{optimum}}$ where $V_{\text{operating}}$ is the diode operating voltage corresponding to the diode optimum operating bias current level, I_{optimum}.

IV. RF PERFORMANCE

A. Optimum Tuning Criteria

Because of the particular circuit application considered, the tuning criterion adopted in all the experimental results reported here was optimum efficiency consistent with high-quality operational output waveforms. For a given diode and bias current, this resulted not in the maximum power but rather in an optimum voltage collapse ratio (i.e., optimum $V_{\text{operating}}/V_{\text{breakdown}}$) condition. This condition has a distinguishable feature in that minimum detected RF leading-edge jitter, relatively noise-free and stable oscillations are *always* obtained for a given bias current level. Tuning for maximum power, on the other hand, was found to result in reduced quality of the output waveforms obtained. In all the tests, a 200-ns pulsewidth was used. However, because of high current densities to which the diodes were subjected, a 0.1-percent duty cycle was employed to minimize possible diode failure due to thermal limitations.

A large number of diodes from several different wafers were tested using the preceding criteria. The diodes had varying diameters (16–33 mil) and different breakdown voltages (160–286 V). The results obtained for increasing bias current, with the circuit retuned at each current level, are similar in characteristics to those shown in Fig. 3 for a 33-mil-diameter diode with depletion layer width of 9 μ and breakdown voltage of 200 V. The optimum voltage collapse ratio considered here for the lumped-element circuit at a given bias current may be regarded as analogous to that in an earlier report [16]. However, no further comparison is possible since the tuning conditions and circuits are different. The optimum voltage collapse ratio of Fig. 3 is seen to possess the following three distinct regions: the low- and high-current collapse regions where the diode efficiency is less than the maximum value, and the minimum constant region where the efficiency reaches its maximum value for a given range of bias currents. Fig. 3 further shows that both the efficiency and leading-edge jitter are dependent on the optimum voltage collapse ratio with the minimum jitter occurring at the state of maximum efficiency and the region of lowest optimum voltage collapse ratio. Significantly too, the frequency of oscillation increases more slowly in the region of optimum voltage collapse ratio than in the other regions, strengthening the conjecture that optimum diode–external circuit interaction conditions exist in that region.

The characteristic operational waveforms and power spectrum corresponding to the region of constant voltage collapse ratio are shown in Fig. 4(a) and (b). The symmetry and the well-defined nulls in the spectrum indicate that minimum leading-edge jitter and noise-free stable TRAPATT oscillations are present.

The behavior of the optimum voltage collapse ratio with increase in bias current is related to diode voltage and conduction current waveforms. Computer results [12] have shown that the diode's most efficient state with increasing drive current is characterized by a well-defined, moderately wide conduction current and by a terminal voltage with a long trapped-plasma duration and fast rise and fall times. In a practical TRAPATT circuit, this condition would correspond to the constant optimum voltage collapse ratio region with the associated maximum diode efficiency. Low-drive current levels were shown to result in short trapped-plasma duration and spiky conduction current waveforms with less efficient plasma generation On the other hand, higher drive current levels than the optimum gave excessive overvoltage (diode peak voltage/breakdown voltage) with the diode voltage exceeding its quiescent value more than once in a cycle, and with the conduction current becoming large and increasingly distorted. The computed efficiencies for these two conditions were lower than the maximum, and hence the present experimentally observed reduced efficiencies.

The values of minimum leading-edge jitter as indicated in Fig. 4(a) were observed to vary from diode to diode

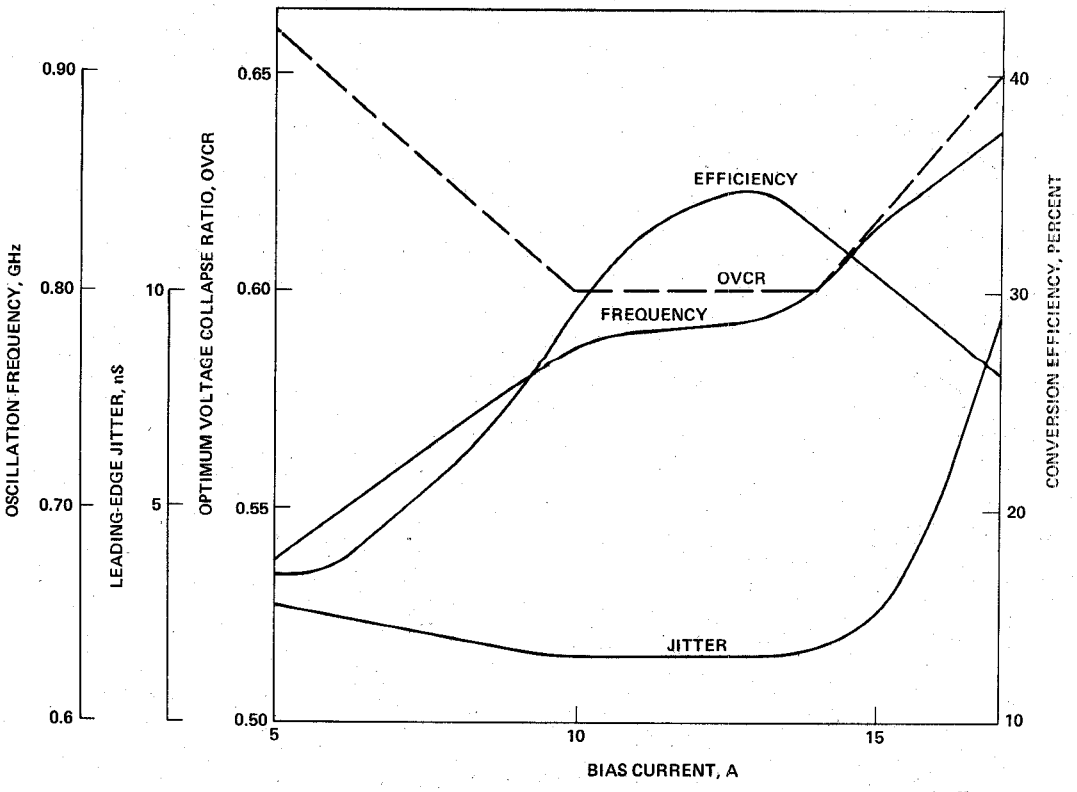


Fig. 3. Typical dc and RF performance for optimally tuned lumped-element TRAPATT oscillator.

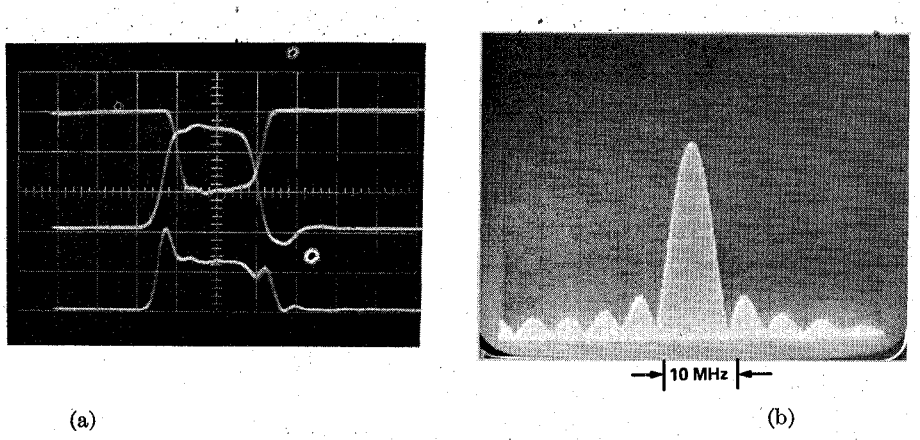


Fig. 4. (a) Operational output waveforms at the minimum optimum voltage collapse ratio region. Top: detected RF pulse—0.1 V/div. Middle: bias current—5 A/div. Bottom: bias voltage—100 V/div. Horizontal scale: 100 ns/div.

for a given oscillator and pulse generator circuits, optimum dc bias circuit, and optimum circuit loading conditions. To date, minimum jitter measured is 0.08 ns from one of our best diode series while the worst jitter is about 20 ns from a relatively nonoptimized diode.

B. Effect of P-Side Width and Diode Diameter on RF Performance

A deep-diffused (highly graded) junction will have varying portions of the depletion width extending into the p-side of the junction depending on material parameters and diffusion conditions. In order to investigate the influence of this variation on diode RF performance, several p^+-n-n^+ TRAPATT diodes from different wafers and with breakdown voltage of 200 V, depletion layer width of approximately 9 μ, diameter 33 mil but with varying width ratio W_P/W_T were fabricated and tested in the same lumped-element circuit of Fig. 2. The optimum tuning criterion described earlier was adopted. The typical results obtained plotted against increasing bias current are shown in Figs. 5 and 6. It is seen that as W_P/W_T increases, the current density, RF power, and maximum efficiency capability of the diodes increase. Powers in excess of 500 W have been consistently obtained from diodes with W_P/W_T greater than 0.4. The optimum oscillation frequencies corresponding to the ex-

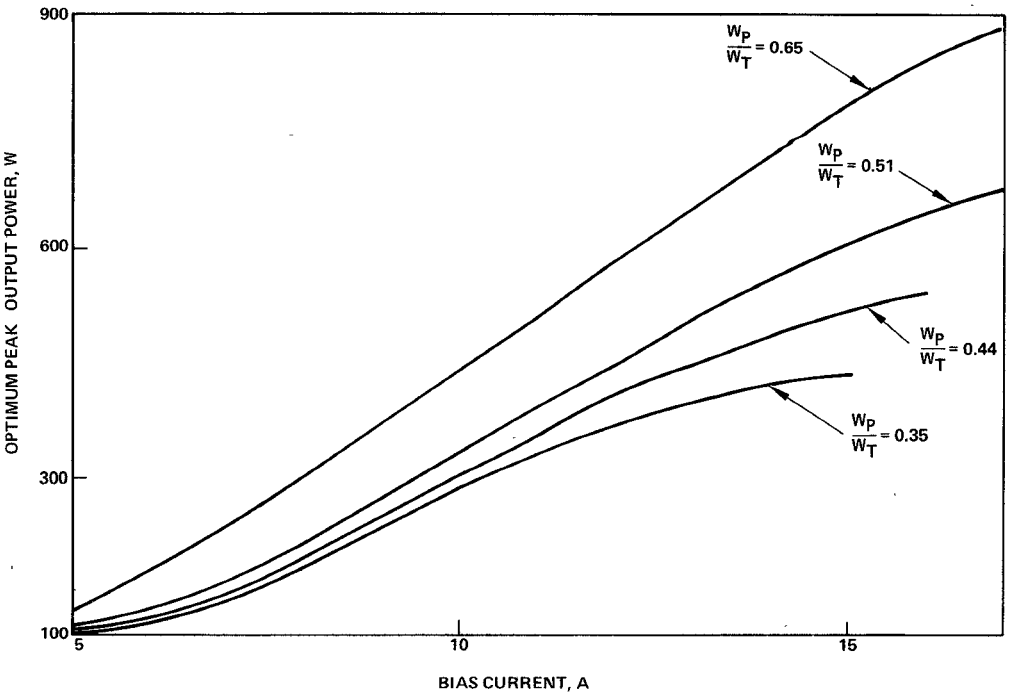


Fig. 5. Output power bias current characteristics for varying diode width ratio W_P/W_T (diode diameter = 33 mil).

tremities and middle-point of the constant optimum voltage collapse ratio region of each diode were measured and plotted as a function of the width ratio as shown in Fig. 6(b) for diodes from five different wafers. Since the diodes had the same area, breakdown voltage, and depletion layer width, one would expect from TRAPATT theory that they should exhibit the same optimum frequency at the optimum efficiency region. Fig. 6(b) shows that this hypothesis is not necessarily true. For width ratios less than 0.5, the optimum oscillation frequency is slightly dependent on the width ratio. However, for width ratios greater than 0.50, a discernible increase in optimum oscillation frequency is obtained. These results suggest that for a given value of the total depletion layer width W_T the optimum oscillation frequency, f_{opt}, for deep-diffused TRAPATT diodes does not necessarily obey the empirical design criterion [17] relating W_T in microns to f_{opt} in gigahertz, $f_{opt} = 7/W_T$, which holds approximately true for abrupt junction devices. This observation has also been reported elsewhere [5]. Rather, for a given deep-diffused diode, $f_{opt} = m/W_T$, where m varies depending on the precise doping profile and, in particular, on the position of the junction with respect to the boundaries of the depletion region.

The foregoing results point out an apparent inherent advantage of deep-diffused p^+-n-n^+ TRAPATT structures, namely that high peak powers are possible from single devices without the complexity of employing multiple-series-connected diodes. Also the results suggest methods of selecting these devices depending on the diode requirements. For high-power and high-current capability, diodes with large width ratios (≥ 0.45) are to be chosen. If optimum operation at relatively low-current densities and lowest optimum oscillation frequency is desired, diodes with width ratios in the neighborhood of 0.4 are to be preferred. Thus there should be a tradeoff between the control of frequency and achieving high performance capability from the diodes.

The minimum optimum voltage collapse ratios corresponding to the maximum efficiencies [dots in Fig. 6(a)] were, respectively, 0.52, 0.54, 0.60, and 0.638 for the increasing width ratio. Since the diodes had the same breakdown voltage, these values lead to the conclusion that the minimum optimum voltage collapse ratio, apart from being a measure of maximum efficiency expected from a TRAPATT diode, is a strong function of both the diode and the test circuit.

A plausible explanation for the improved performance of deep-diffused p^+-n-n^+ TRAPATT structures with increase in width ratio may be obtained by considering the structure as behaving electrically like two diodes in series (p^+-p-n and p-n-n^+). The result is an increase in the diode impedance which in turn allows large area diodes to be used to produce higher peak powers. For width ratios, $0 < W_P/W_T < 0.5$, the structure could constitute a type of n-type "double-drift" TRAPATT diode possessing performance superiority over the corresponding abrupt junction diode ($W_P/W_T = 0$) as has been shown for the case of IMPATT diodes [18], [19]. However, as $W_P/W_T \rightarrow 1$ (i.e., the metallurgical junction moves closer to the n^+ region), the situation changes as the diode could now be regarded as behaving more like a complementary p-type deep-diffused TRAPATT structure with its inherent higher performance capability over the corresponding n-type TRAPATT structure [20], [21].

In order to investigate the effect of diode diameter on

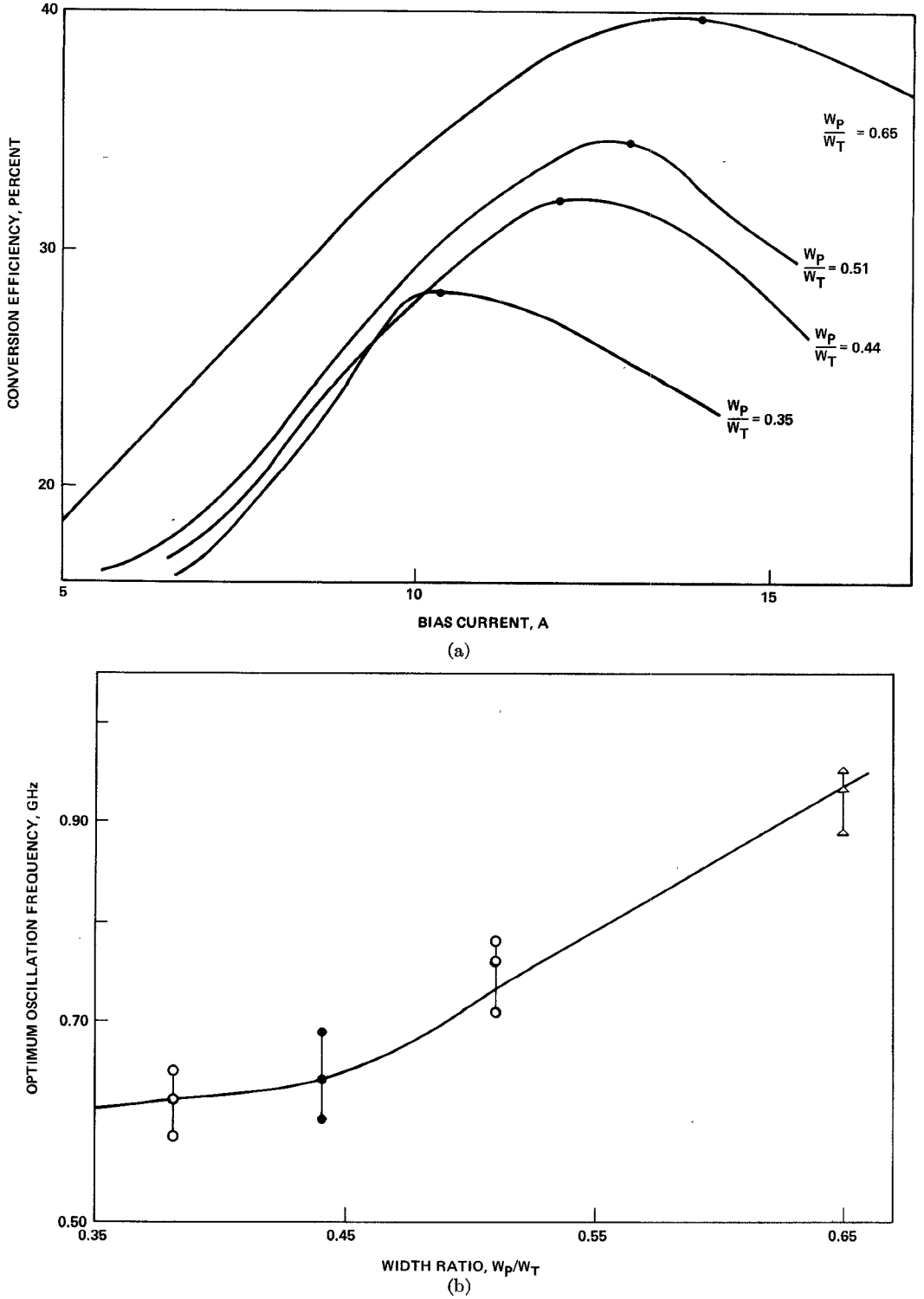


Fig. 6. (a) Conversion efficiency–bias current characteristics for varying diode width ratio W_P/W_T (diode diameter = 33 mil). (b) Optimum oscillation frequency versus diode width ratio W_P/W_T.

RF performance, several diodes from different wafers were tested. Diodes from the same wafer had the same characteristics such as the same doping profile, breakdown voltage, depletion layer width W_T, and doping density N_D, and the same width ratio W_P/W_T but different diameters. Diodes from different wafers had breakdown voltages varying from 160–225 V and N_DW_T from 49.4 $\times$ 10^{10} to 100 $\times$ 10^{10} cm^{-2}. For each diode, the optimum tuning criterion was employed to determine the frequency and power at the maximum efficiency. The larger diameter diodes were observed to give higher output powers as might be expected. It was also further observed that the current density at the maximum efficiency increases with the diode area. Fig. 7 shows the results obtained for diodes from four different wafers. The operating frequency is shown to decrease with increase in the diode diameter.

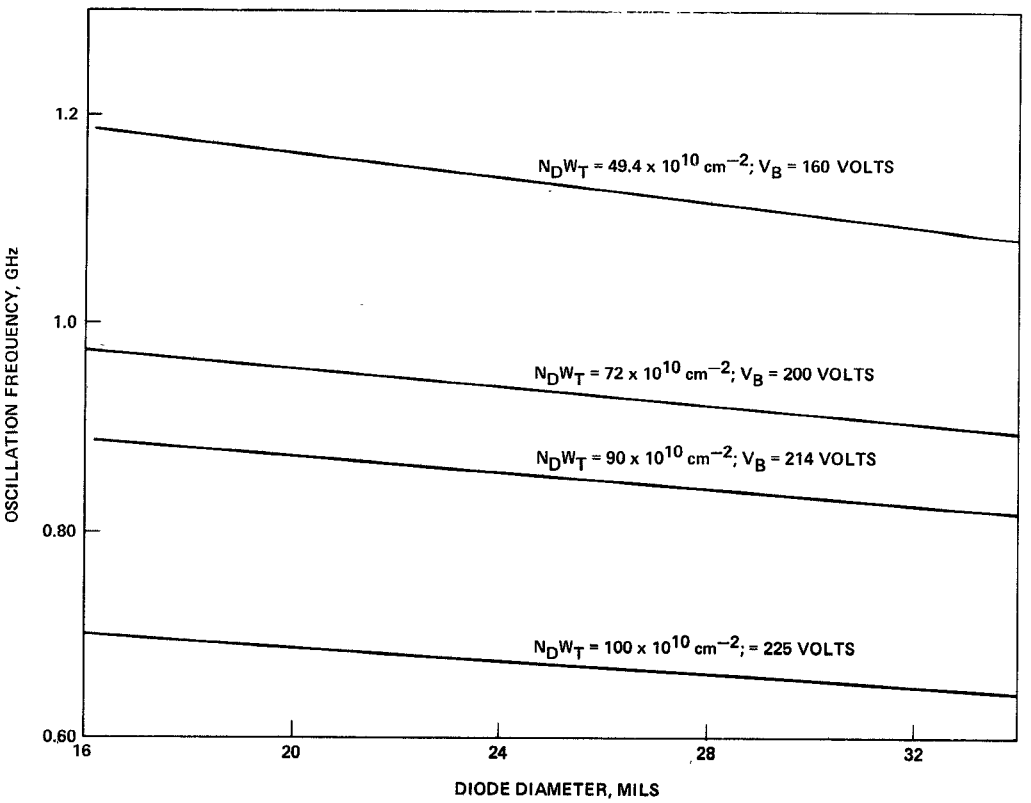


Fig. 7. Oscillation frequency versus diode diameter.

A possible explanation for the lower frequency of oscillation observed for larger diameter diodes may lie in the magnitude of the diode current density. Computer results [12] have shown that, even though avalanching may be taking place throughout the depletion layer width for terminal current levels higher than the critical value, the effective avalanching width for a given TRAPATT diode is an increasing function of the current density. Thus in an actual TRAPATT circuit, the effective avalanching width rather than the nominal depletion layer width could be an important frequency controlling parameter, and hence the observed results.

C. Effect of Critical Circuit Elements on Oscillator Performance

Some of the critical circuit elements affecting the designed lumped-element TRAPATT oscillator performance have been investigated. Since the externally introduced circuit inductance contacting the packaged diode is in series with the diode, the total effective series inductance in the vicinity of the active device can be controlled by varying this contacting inductance. For a fixed bias current, the total inductance was varied from the predicted optimum value with the circuit retuned for the best operation possible. Typical performance characteristics obtained are shown in Fig. 8 for a 28-mil-diameter diode with a breakdown voltage of 200 V. It is seen that the RF output power exhibits an approximately linear increase until a maximum value is reached and then falls sharply with further inductance increase beyond the optimum value. Results from several other diodes with varying areas and breakdown voltages but in packages with the same parasitics showed that the optimum series inductance is approximately the same irrespective of the diode tested. Also the higher the inductance above the optimum value, the more difficult it was to obtain clean diode switching in the circuit as typified by the output waveforms. Furthermore, changing the package inductance by varying the number of the diode-package connecting ribbon leads, resulted in similar deterioration of oscillation performance [7]. However, in this case, the package inductance effect can be offset by also varying the external inductance.

These results lead to the conclusions that the package and the externally introduced inductances act as an effective series inductance in the vicinity of the diode, and that a moderate amount of this total effective series inductance is necessary for optimum performance in a practical lumped-element TRAPATT circuit.

The results obtained and the conclusions reached in the preceding paragraphs agree with the theoretical predictions from different TRAPATT computer models [11], [22]. For optimum TRAPATT operation, the triggering waveform originating from the active device must remain undistorted as it interacts with the external circuit. It has been shown theoretically [22] that too little or too large a package inductance causes high- or low-frequency "ringing" in the quiescent portion of the voltage waveform, and that these effects are detrimental to efficient TRAPATT operation. On the other hand, computer results from the diode-physics–external circuit interaction analysis [11] have

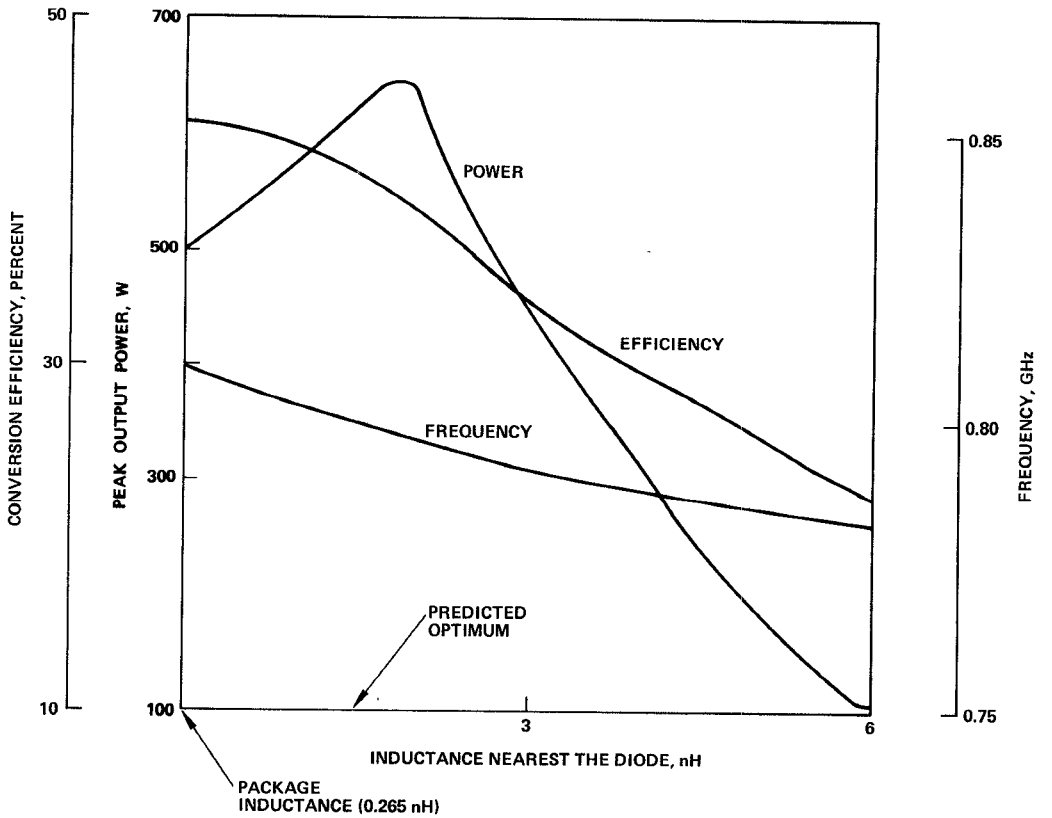


Fig. 8. TRAPATT oscillator performance versus inductance nearest the diode (diode diameter = 28, I_{bias} = 12 A).

shown that large values of the *total effective series inductance* closest to the diode not only excite large amplitude transients in the quiescent portion of the voltage waveform but may also cause large amplitude distortion during the high conducting state of the diode. The overall effect is the deterioration in the performance and decrease in operating frequency observed in this investigation.

The beneficial effect of an extra charging capacitance in the immediate vicinity of the diode has been observed by Evans [8] for TRAPATT diodes operating in a conventional slug-tuned coaxial circuit. Subsequent studies [23], [16] have confirmed this observation. In the lumped-element circuit considered, no significant electrical length separates one element from another or from the diode. In addition, all the tuning capacitances together with the package and diode active region capacitances are in parallel. It would appear, therefore, that the total oscillator capacitance and hence the effective circuit *RC* time constant could be controlled to the same degree by varying any of the tuning capacitances. Thus the extent of influence of the capacitors on the oscillator performance would be expected to be the same. The results obtained for a fixed bias current are shown in Fig. 9. The capacitances were varied one at a time above and below their predicted optimum values to obtain the corresponding curves. It is seen that, although the capacitances produce similar control on the oscillator performance, the variation of the capacitance in the immediate diode vicinity has a more critical influence on the RF performance. This is shown more clearly in Fig. 9(b). Similar results obtained by testing different diodes showed that the optimum values of the capacitances varied depending on the diode and breakdown voltage. In all cases, too small a capacitance resulted in poor quality operational output waveforms with the detected RF pulse frequency hardly measurable with the frequency meter. The circuit is said to be unable to sustain the harmonics necessary for efficient TRAPATT operation, and hence the degradation in the oscillator performance obtained. On the other hand, for large values of the circuit capacitance, the operational output waveforms were observed to be of relatively high quality but with substantially reduced detected RF pulse present. This implies that most of the harmonic power including a substantial fraction of the fundamental power was efficiently trapped in the circuit with the consequent deterioration in performance.

D. Circuit Frequency Tunability and Diode Adaptability

It has been shown earlier that an optimum circuit condition corresponding to an optimum voltage collapse ratio exists for a fixed bias current. Therefore, for a given bias current, the oscillator could be tuned about this optimum operating point in order to obtain the circuit frequency tunability. Fig. 10 shows typical frequency tunability of the lumped-element circuit obtained for diodes designed to oscillate in UHF and lower *L* band frequency ranges, respectively, and fabricated from two different wafers.

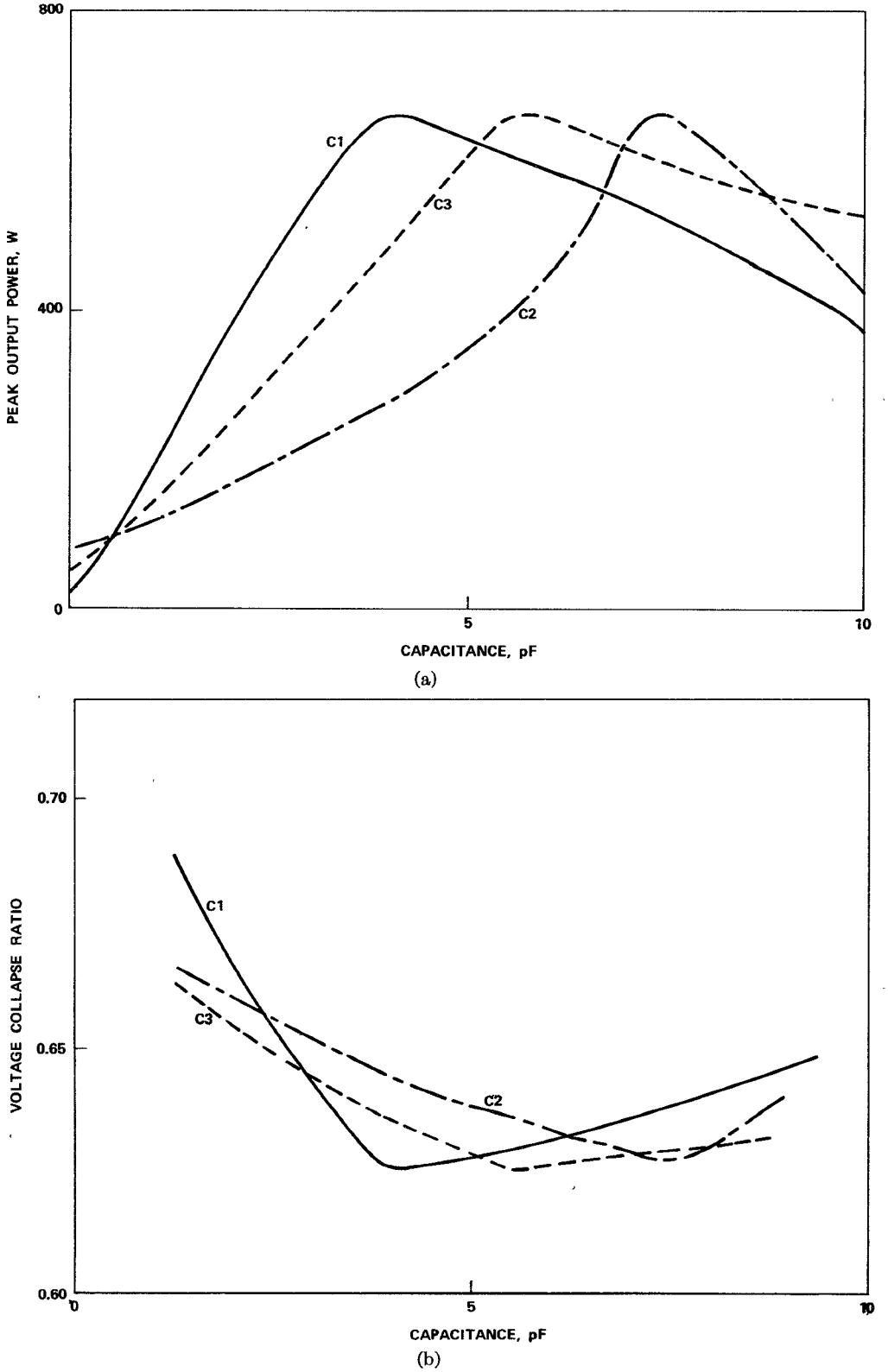


Fig. 9. (a) Effect of circuit capacitance on output power (diode diameter = 28 mil, I_{bias} = 12 A). (b) Voltage collapse ratio versus circuit tuning capacitances (diode diameter = 28 mil, I_{bias} = 12 A).

The extremities of the tuning range were characterized by a detected RF signal whose frequency could not easily be determined with the frequency meter. Results from several diodes tested have shown that a minimum of 35-percent frequency tunability was easily obtained at any given bias current.

In the coaxial TRAPATT circuit, the operating frequency is primarily determined by the position of a filter approx-

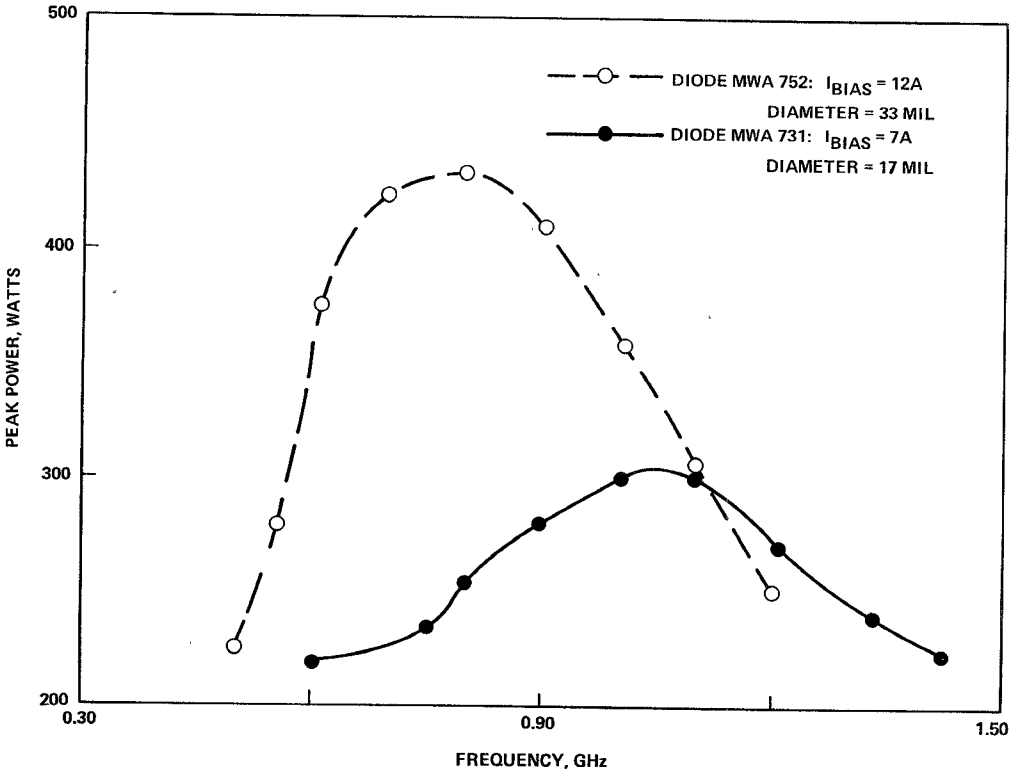


Fig. 10. Frequency tunability and diode adaptability of a lumped-element TRAPATT oscillator circuit.

imately a half-wavelength away from the diode. The lumped-element circuit does not suffer from such a restriction. Thus, provided that a lumped-element TRAPATT circuit is well designed, its tuning capability should be such as to provide optimum performance for diodes of different characteristics and designed to operate at different frequency bands. Fig. 10 illustrates the case for typical UHF and typical lower L band diodes.

V. CONCLUSIONS

The design and performance of a lumped-element TRAPATT oscillator utilizing deep-diffused p^+-n-n^+ silicon diodes designed primarily for solid-state pulsed radar applications in the UHF and lower L band frequency ranges have been discussed. It has been shown that the performance capability of deep-diffused TRAPATT diodes can be enhanced by exploiting the relative position of the junction in the device depletion region. Optimum circuit tuning criteria for minimum detected RF leading-edge jitter, noise-free and stable oscillations in a given circuit have been demonstrated. Some of the critical circuit elements influencing the RF performance of a lumped-element TRAPATT circuit have been investigated. A frequency tuning range of at least 35 percent has been shown to be possible with a lumped-element circuit.

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Satellite Altimetry Applications

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Abstract—**This paper provides a brief background of precision satellite altimetry. A description of satellite altimetry concepts and instrumentation is presented. The parameters measured, supporting data, and techniques, as well as physical limitations, are discussed. In addition, results are shown and a variety of applications is emphasized.**

INTRODUCTION AND BACKGROUND

SATELLITE altimetry is primarily devoted to active sensing of the ocean-surface topography which is then utilized for geodetic and oceanographic studies.

The long-term objectives of satellite altimetry were stated in the 1969 Williamstown study on Solid Earth and Ocean Physics [1] and the 1972 Earth and Ocean Physics Applications Program (EOPAP) report. These studies call for development of a 10-cm-accurate synoptic satellite altimeter with at least 1° (100-km) spatial resolution.

SATELLITE ALTIMETRY CONCEPT

The basic idea behind altimetry is to utilize the highly stable platform provided by a satellite as a moving reference system from which vertical measurements to the ocean surface are made (see Fig. 1). The altimeter measures to the instantaneous electromagnetic mean sea level (IEMSL) averaged over the spatial footprint of the instrument.

The IEMSL can be related to the mean sea level (MSL) if the relationship between the radar mean return point, and mean sea height is known. However, MSL often varies because of currents, tides, storm surges, etc. Most of these dynamic ocean effects can be removed if observations are taken over an extended time. The residual steady-state ocean surface topography is directly related to the shape of the geoid.

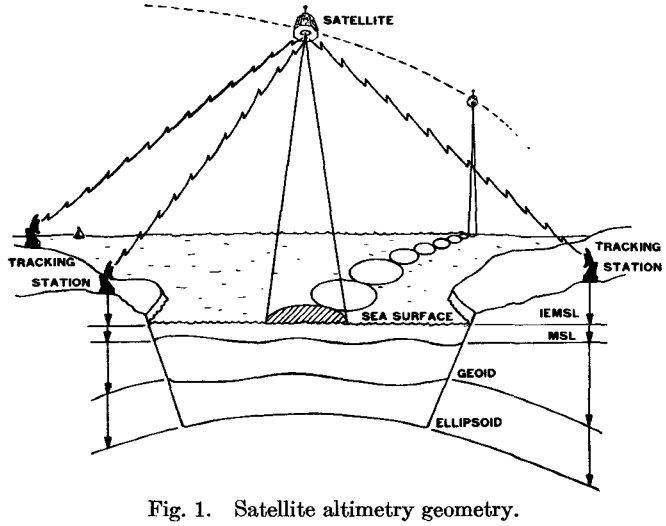

Fig. 1. Satellite altimetry geometry.

INSTRUMENTATION

The Skylab radar altimeter was the first in a series of satellite altimeters that are planned to progressively achieve the EOPAP goals. This altimeter was designed primarily for obtaining the radar technology for designing improved altimeters. Currently, the GEOS-C altimeter launched April 9, 1975, will be the first globally applied system. In 1978 the SEASAT-A altimeter will be a part of an ocean-dedicated satellite instrumentation system and will be the first attempt to achieve 10-cm resolution [2]. A comparison of these satellite systems is presented in Table I.

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